Docket No. 1514.1010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Woo Young SO et al.

Serial No. 10/068,004 Group Art Unit: 2826

Confirmation No. 6442

Filed: February 8, 2002 Examiner: Ahmed N. Sefer

For: THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF, AND ACTIVE MATRIX DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

SUBMISSION OF ENGLISH TRANSLATION OF PRIORITY DOCUMENT

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Sir:

Pursuant to 37 CFR 1.55(a)(4) and MPEP 201.15, attached hereto are an English translation of Korean Application No. 2001-10842 filed on March 2, 2001, and a statement that the English translation is accurate to perfect the applicants' claim for foreign priority under 35 USC 119(a)-(d). A certified copy of the Korean priority application was submitted on March 7, 2002, and receipt of the certified copy was acknowledged by the Examiner in the Office Action of December 4, 2002.

If there are any fees associated with filing of this paper, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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VERIFICATION OF TRANSLATION

I, Woo-Hyun HWANG, of Suite 1810, Hwanghwa Bldg., 832-7, Yeoksam-dong, Gangnam-gu, Seoul, Republic of Korea hereby declare that I am knowledgeable in the English and Korean languages, and that to the best of my knowledge the attached document is a true and complete English translation of Korean Patent Application No. 10-2001-0010842.

Dated April 13, 2006

Woo-Hyun Hwang

Signature

Translation of Priority Document

THE KOREAN INTELLECTUAL PROPERTY OFFICE

This is to certify that annexed hereto is a true copy from the records of the Korean Intellectual property Office of the following application as filed

Application Number : Korean Patent Application No. 2001-10842

Date of Application : March 2, 2001

Applicant(s) : Samsung SDI Co., Ltd.

May 7, 2001

COMMISSIONER

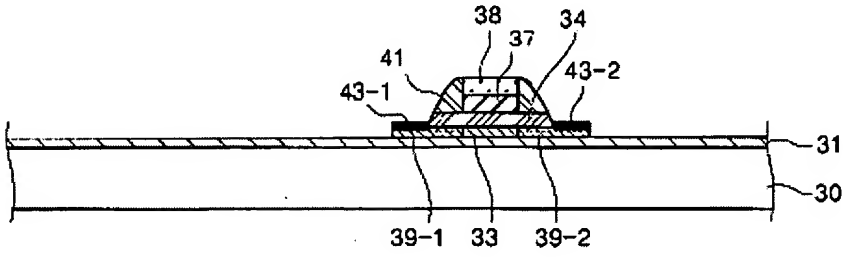
[Abstract of the Disclosure]

[Abstract]

Provided are a thin film transistor (TFT) and a method of manufacturing the TFT wherein source and drain electrodes contact source and drain regions without contact holes. The method includes: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; implanting high-concentration impurity ions into the exposed semiconductor layer and forming high-concentration source and drain regions; and forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

[Typical Figure]

FIG. 3I



[Specification]

[Title of the Invention]

THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF, AND ACTIVE MATRIX DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

[Brief Description of the Drawings]

FIGS. 1A to 1E are cross-sectional views illustrating a conventional process of manufacturing a TFT;

FIGS. 2A to 2D are cross-sectional views illustrating a conventional method of manufacturing an OLED;

FIGS. 3A to 3L are cross-sectional views illustrating a method of manufacturing a thin film transistor (TFT) according to an exemplary embodiment of the present invention;

FIG. 4 is a circuit diagram of an OLED according to the exemplary embodiment of the present invention;

FIG. 5 is a plan view of the OLED of FIG. 4;

FIGS. 6A to 6Q are cross-sectional views taken along line A-A` of FIG. 5;

FIGS. 7 and 8 illustrate another example forming a contact for electrically connecting a drain electrode of a TFT to an anode of an organic EL diode in the method of manufacturing the OLED according to an exemplary embodiment of the present invention; and

FIG. 9 is a cross-sectional view illustrating another modification of the contact hole through which the pixel electrode contacts either of the source and drain electrodes.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a thin film transistor (TFT) and a method of manufacturing the TFT wherein source and drain electrodes contact source and drain regions without contact holes. Also, the present invention relates to an active matrix display device and a manufacturing method manufacturing the same using a TFT having a non-contact hole structure.

As a flat panel display device, an organic EL display device is being watched with keener interest than other display device such as a cathode ray tube (CRT) and a liquid crystal display (LCD) device. In comparison to the CRT having the same screen size, the organic EL display device is thin, lightweight, and low in power consumption. Since the organic EL display device emits light by itself, it does not require a back light device. Therefore, a lightweight, small-sized and compact display device can be achieved. In addition, the organic EL display device has an advantage in that there is no limitation to a viewing angle.

Recently, the organic EL display device having a thin film transistor (TFT) as a switching device is being actively developed.

FIGS. 1A to 1E are cross-sectional view illustrating a conventional process of manufacturing a TFT.

Referring to FIG. 1A, a buffer layer 11 is formed on a transparent insulating substrate 10. The substrate is a transparent glass substrate or a transparent plastic substrate. A polycsilicon layer is deposited on the buffer layer 11 and then patterned to form a semiconductor layer 12.

Then, as shown in FIG. 1B, a gate insulating layer 13 is deposited on the

entire surface of the substrate 10 and covers the semiconductor layer 12. The gate insulating layer 13 serves as a gate insulating layer. A first metal layer is deposited on the gate insulating layer 13 over the semiconductor layer 12 and then patterned to form a gate electrode 14.

Using the gate electrode 14 as a mask, low-concentration impurity ions, for example, n-type or p-type low-concentration impurity ions are implanted into the semiconductor layer 12 to form low-concentration source and drain regions 15-1 and 15-2.

Thereafter, as shown in FIG. 1C, the gate electrode 14 is anodized to form an anodizing layer 16. When the gate electrode 14 is formed of aluminium (Al), the anodizing layer is formed of Al_2O_3.

High-concentration impurity ions having the same conductivity as the low-concentration source and drain regions 15-1 and 15-2 are implanted into the semiconductor layer 12 to form high-concentration source and drain regions 17-1 and 17-2.

Subsequently, as shown in FIG. 1D, an interlayer insulating layer 18 is deposited on the entire surface of the substrate 10 and the interlayer insulating layer 18 and the gate insulating layer 13 are etched such that the high-concentration source and drain regions 17-1 and 17-2 are exposed, thereby forming contact holes 19-1 and 19-2.

A metal layer is formed on the interlayer insulating layer 18 having the contact holes 19-1 and 19-2 and then patterned to form source and drain electrodes 20-1 and 20-2 contacting the high-concentration source and drain regions 17-1 and 17-2 through the contact holes 19-1 and 19-2. Accordingly, the conventional TFT

having a lightly doped drain (LDD) structure of the low-concentration source and drain regions 15-1 and 15-2 and the high-concentration source and drain regions 17-1 and 17-2 is completed.

Meanwhile, in order to manufacture the TFT having an off-set structure, the process of implanting the low-concentration impurity ions is omitted.

In order to manufacture the TFT having the LDD structure or the off-set structure, four mask processes are required: a first mask to form the semiconductor layer 12; a second mask to form the gate electrode 14; a third mask to form the contact holes 19-1 and 19-2; and a fourth mask to form the source and drain electrodes 20-1 and 20-2. Therefore, a manufacturing process is very complicated, and a production cost is high.

Also, the conventional method of manufacturing the TFT uses the anodizing layer other than a photoresist pattern and thus forms the LDD region in a self-align manner. However, an additional apparatus is necessary to anodize the gate electrode and form the anodizing layer, leading to a very complicated manufacturing process.

In addition, since the source and drain electrodes, without contact holes, contact the high-concentration source and drain regions, contact resistance increases, thereby degrading electric characteristics of the TFT.

FIGS. 2A to 2D are cross-sectional view illustrating a process of manufacturing an organic EL display device having the TFT of FIG. 1E as a switching device.

Subsequent to FIG. 1E, a third insulating layer 21 is formed on the entire surface of the substrate 10 and covers the source and drain electrodes 20-1 and 20-

2 as shown in FIG. 2A. The third insulating layer 21 serves as a passivation layer. The passivation layer 21 includes a third contact hole 22 at a location corresponding to a portion of either of the source and drain electrodes 20-1 and 20-2. In FIG. 1E, the third contact hole 20 is formed on a portion of the drain electrode 20-2.

Then, as shown in FIG. 2B, a transparent conductive material is deposited and then patterned to form a pixel electrode 23. The pixel electrode 21 contacts the drain electrode 20-2 through the third contact hole 22 and serves as an anode electrode.

Subsequently, as shown in FIG. 2C, a planarization layer 24 is formed on the entire surface of the substrate 10. The planarization layer 24 has an opening portion 25. The opening portion 23 exposes a portion of the pixel electrode 23.

Next, as shown in FIG. 2D, an organic EL layer 26 is formed on the exposed portion of the anode electrode 23, and thereafter a cathode electrode 27 is formed to cover the organic EL layer 26. Therefore, the organic EL display device is completed.

In order to manufacture the organic EL display device, three mask processes are required in addition to a four-mask process to manufacture the TFT: a fifth mask to form the third contact hole; a sixth mask to form the anode electrode; and a seventh mask to form the opening portion 25.

Therefore, process number and processing time increase, and a manufacturing process is very complicated. As a result, a manufacturing yield is low, and a production cost is high.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide a TFT, a method of

fabricating the same, an active matrix type display device using the same, and a method of fabricating the same, which forms a Lightly Doped Drain (LDD) structure or an offset structure in a self-alignment manner to simplify a process thereof and ensure a process margin.

It is another object of the invention to provide a TFT, a method of fabricating the same, an active matrix type display device using the same, and a method of fabricating the same, which forms an LDD structure or an offset structure using spacers to simplify a process.

It is still another object of the invention to provide a TFT having an LDD structure or an offset structure, a method of fabricating the same, an active matrix type display device using the same, and a method of fabricating the same, which has source and drain electrodes in direct contact with source and drain regions without contact holes to simplify a process.

It is yet another object of the invention to provide a TFT having an LDD structure or an offset structure, a method of fabricating the same, and a method of fabricating an active matrix type display device using the same, which can reduce contact resistance of source and drain electrodes.

It is yet another object of the invention to provide a TFT, a method of fabricating the same, an active matrix type display device using the same, and a method of fabricating the same, that are capable of reducing contact resistance by forming a silicide layer on source and drain regions, enhancing an etch selectivity at the time of forming source and drain electrodes to ensure a process margin, and preventing a semiconductor layer from being damaged at the time of implanting high-concentration impurity ions.

It is yet another object of the invention to provide a TFT, a method of fabricating the same, and an active matrix type display device using the same, which surrounds a gate with a capping material to prevent the gate from being damaged at the time of implanting impurity ions for forming source and drain regions.

[Construction of the Invention]

In one aspect, the invention is directed to a method of fabricating a TFT, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; implanting high-concentration impurity ions into the exposed semiconductor layer and forming high-concentration source and drain regions; and forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

In another aspect, the invention is directed to a method of fabricating a TFT, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; forming a silicide layer on the exposed semiconductor layer; implanting high-concentration impurity ions into the semiconductor layer below the silicide layer, and forming high-concentration source and drain regions having an offset structure spaced apart from the gate by a

predetermined interval; and forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

In still another aspect, the invention is directed to a method of fabricating a TFT, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask to form low-concentration source and drain regions; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; forming a silicide layer on the exposed semiconductor layer; forming an LDD structure by implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the semiconductor layer below the silicide layer and forming high-concentration source and drain regions; and forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

In yet another aspect, the invention is directed to a TFT, comprising: a semiconductor layer disposed on an insulating substrate; a gate insulating layer disposed on the semiconductor layer to expose both sides of the semiconductor layer; a gate disposed on the gate insulating layer; a gate capping layer disposed on the gate; a spacer disposed on sidewalls of the gate capping layer and the gate on the gate insulating layer; high-concentration source and drain regions disposed in the exposed semiconductor layer; and source and drain electrodes in direct contact with the high-concentration source and drain regions.

In yet another aspect, the invention is directed to a method of fabricating an active matrix display device, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; implanting high-concentration impurity ions into the exposed semiconductor layer, and forming high-concentration source and drain regions having an offset structure spaced apart from the gate by a predetermined interval; forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask; forming a planarization layer on the entire surface of the substrate; etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole; and forming a pixel electrode on an interlayer insulating layer including the contact hole using a fifth mask.

In yet another aspect, the invention is directed to a method of fabricating an active matrix display device, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask and forming low-concentration source and drain regions; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; forming an LDD structure by implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the exposed

semiconductor layer and forming high-concentration source and drain regions; forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask; forming a planarization layer on the entire surface of the substrate; etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole; and forming a pixel electrode on an interlayer insulating layer including the contact hole using a fifth mask.

In yet another aspect, the invention is directed to a method of fabricating an active matrix display device, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate having a gate capping layer on the gate insulating layer using a second mask; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; forming a silicide layer on the exposed semiconductor layer; Implanting high-concentration impurity ions into the semiconductor layer below the silicide layer to form high-concentration source and drain regions having an offset structure that is spaced apart from the gate by a predetermined interval; forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask; forming a planarization layer on the entire surface of the substrate; etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole; forming an anode electrode on an interlayer insulating layer including the contact hole using a fifth mask; forming an organic thin layer on the anode electrode; and forming a cathode electrode on the organic thin layer.

In yet another aspect, the invention is directed to a method of fabricating an active matrix display device, comprising: forming a semiconductor layer on an insulating substrate using a first mask; forming a gate insulating layer on the insulating substrate including the semiconductor layer; forming a gate and a gate capping layer on top of the gate on the gate insulating layer on the semiconductor layer using a second mask; implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask and forming low-concentration source and drain regions; forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer; forming a silicide layer on the exposed semiconductor layer; forming a lightly doped drain (LDD) structure by implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the semiconductor layer below the silicide layer and forming high-concentration source and drain regions; forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask; forming a planarization layer on an entire surface of the substrate; etching the planarization layer and exposing any one of the source and drain electrodes using a fourth mask to form a contact hole; forming an anode electrode on an intermediate insulating layer including the contact hole using a fifth mask; forming an organic thin layer on the anode electrode; and forming a cathode electrode on the organic thin layer.

In yet another aspect, the invention is directed to an active matrix display device, comprising: a gate line and a data line crossing each other and arranged on an insulating substrate; a power supply line crossing the gate line and arranged parallel to the data line; and a pixel disposed in a pixel region defined by the gate line,

the data line, and the power supply line, the pixel including: a first thin film transistor (TFT) having a first gate, a first semiconductor layer, and first source and drain electrodes; a second TFT having a second gate, a second semiconductor layer, and second source and drain electrodes; a capacitor having first and second electrodes; and a pixel electrode, wherein the first source and drain electrodes of the first TFT are in direct contact with the first semiconductor layer, one of the first source and drain electrodes is connected to the first electrode of the capacitor through a connection pad, the second source and drain electrodes of the second TFT are in direct contact with the second semiconductor layer, and one of the second source and drain electrodes is in contact with the pixel electrode through a contact hole.

In yet another aspect, the invention is directed to an active matrix display device comprising a gate line and a data line crossing each other and arranged on an insulating substrate, a power supply line crossing the gate line and arranged parallel to the data line, and a pixel disposed in a pixel region defined by the gate line, the data line and the power supply line and having first and second thin film transistors (TFT), a capacitor, and a pixel electrode, the active matrix display device comprising: a first semiconductor layer of the first TFT and a second semiconductor layer of the second TFT disposed on the insulating substrate; first and second gate insulating layers disposed on the first and second semiconductor layers to expose both sides of the respective first and second semiconductor layers, and a third gate insulating layer disposed on the substrate; first and second gates of the first and second TFTs, the first and second gates having first and second capping layers thereon and disposed on the first and second gate insulating layers, respectively; a first electrode of the capacitor having a dielectric layer thereon and disposed on the

third gate insulating layer; a spacer disposed on sidewalls of the first electrode of the capacitor and the first and second gates of the first and second TFTs; a high-concentration source region of the first TFT disposed in the exposed first semiconductor layer and a high-concentration source region of the second TFT disposed in the exposed second semiconductor layer; first and second source and drain electrodes of the first and second TFTs respectively disposed on the substrate and in direct contact with the first and second source and drain regions; a second electrode of the capacitor disposed on the dielectric layer of the capacitor; a planarization layer having first and second contact holes exposing respective ones of the first and second source and drain electrodes of the respective first and second TFTs, and a third contact hole exposing the first electrode of the capacitor; a pixel electrode connected to one of the second source and drain electrodes of the second TFT through the first contact hole on the planarization layer; and a connection pad disposed to connect one of the first source and drain electrodes of the first TFT to the first electrode of the first capacitor through the respective second and third contact holes on the planarization layer.

In yet another aspect, the invention is directed to a method of fabricating an active matrix display device comprising a gate line and a data line crossing each other and arranged on an insulating substrate, a power supply line crossing the gate line and arranged parallel to the data line, and a pixel formed in a pixel region defined by the gate line, the data line and the power supply line, the pixel having first and second thin film transistors (TFT), a capacitor, and a pixel electrode, the method comprising: forming a first semiconductor layer of a first thin film transistor (TFT) and a second semiconductor layer of a second TFT on the substrate using a first mask;

forming a gate insulating layer on the substrate including the first and second semiconductor layers; forming first and second gates including respective first and second gate capping layers on the gate insulating layer of the respective first and second semiconductor layers, a first electrode of the capacitor including a dielectric layer on the gate insulating layer, and the gate line using a second mask; forming a spacer on a sidewall of the first electrode and sidewalls of the first and second gates and simultaneously exposing the first and second semiconductor layers; forming first high-concentration source and drain regions of the first TFT in the exposed first semiconductor layer, and second high-concentration source and drain regions of the second TFT in the exposed second semiconductor layer; forming first source and drain electrodes in direct contact with the first high-concentration source and drain regions, second source and drain electrodes in direct contact with the second high-concentration source and drain regions, a second electrode of the capacitor on the dielectric layer, and the data line and the power supply line on the substrate using a third mask; forming a planarization layer on the entire surface of the substrate; etching the planarization layer and forming a first contact hole exposing one of the first high-concentration source and drain regions, a second contact hole exposing one of the second high-concentration source and drain regions, and a third contact hole exposing the first electrode of the capacitor using a fourth mask; and forming a pixel electrode connected to one of the first high-concentration source and drain regions through the first contact hole, and a connection pad connecting one of the second high-concentration source and drain regions to the first electrode of the capacitor through the second and third contact holes using a fifth mask.

The present invention will now be described more fully hereinafter with reference to attached drawings, wherein the same numerals denote the same components.

FIGS. 3A to 3L are process cross-sectional views illustrating a method of fabricating a thin film transistor in accordance with embodiments of the present invention.

FIGS. 3A and 3B are processes for forming a semiconductor layer on a substrate, which forms a SiO_2 layer 31 as a buffer layer on a transparent substrate 30, and forms then a polysilicon layer 32 thereon. In this case, the method of forming the polysilicon layer 32 may include depositing an amorphous silicon layer and crystallizing it into polysilicon by a predetermined annealing process, or may include directly depositing a polysilicon layer.

Subsequently, the polysilicon layer is patterned using a first mask (not shown) for forming the semiconductor layer. Accordingly, a semiconductor layer 33 is formed on the buffer layer 31.

The buffer layer 31 acts to prevent impurities such as sodium ions generated on an insulating substrate from flowing into the semiconductor layer 33.

FIGS. 3C and 3D illustrate processes for forming a gate, which includes sequentially forming a gate insulating layer 34, a gate electrode material 35, and a gate capping material 36 on the buffer layer 31 having the semiconductor layer 33. In this case, SiO_2 or SiNx is employed as the gate insulating layer 34 and the gate capping material 36.

Subsequently, although not shown in the Figures, the gate capping material 36 and the gate electrode material 35 are sequentially etched using a second mask

for forming a gate to form a gate 37 and a gate capping layer 38 on the gate insulating layer 34 above the semiconductor layer 33.

FIG. 3E illustrates a process for forming low-concentration source and drain regions, which implants low-concentration impurities having a predetermined conductivity type, e.g., p-type or n-type low-concentration impurities into the semiconductor layer 33 using the gate 37 as a mask. Accordingly, low-concentration source and drain regions 39-1 and 39-2 are formed in the semiconductor layer 33 at both sides of the gate 37.

In this case, the gate capping layer 38 is formed on the gate 37 to prevent the low-concentration impurities for the source and drain regions 39-1 and 39-2 from flowing into the gate 37, so that defects such as hillock or crack can be prevented from occurring on the gate 37.

FIGS. 3F and 3G illustrate processes for forming spacers at sidewalls of the gate 37, which includes depositing an insulating layer 40 for a spacer, e.g., a SiO_2 layer or an SiNx layer on the gate insulating layer 34 having the gate 37, and etching back the insulating layer 40 to form spacers 41 on both sidewalls of the gate 37.

In this case, the gate insulating layer 34 below the insulating layer 40 is also etched when the insulating layer 40 for forming the spacer 41 is etched, thereby exposing the low-concentration source and drain regions 39-1 and 39-2.

FIGS. 3H and 3I illustrate processes for forming a silicide layer on the exposed low-concentration source and drain regions 39-1 and 39-2, which includes depositing a metal layer 42 having a high melting point over the entire surface of the substrate and carrying out a silicidation process thereon so that silicon of the semiconductor layer 33 reacts with the metal layer 42. Accordingly, the silicide

layers 43-1 and 43-2 are formed only on portions where the low-concentration source and drain regions 39-1 and 39-2 are exposed and the metal layer 42 still remains in the rest of regions.

Accordingly, when the remaining metal layer 42 is removed, the silicide layers 43-1 and 43-2 are formed only in the low-concentration source and drain regions 39-1 and 39-2. In this case, when a chrome or nickel layer is employed as the high melting point metal layer 42, the silicide layers 43-1 and 43-2 become chrome silicide layers or nickel silicide layers.

FIG. 3J illustrates a process for forming high-concentration source and drain regions, which includes implants impurity ions having the same conductivity as the low-concentration source and drain regions 39-1 and 39-2 into the semiconductor layer using the gate 37 and the spacer 41 as masks to form high-concentration source and drain regions 44-1 and 44-2 in the semiconductor layer below the silicide layers 43-1 and 43-2 in a self-alignment manner. Accordingly, the source and drain regions have a Light Doped Drain (LDD) structure composed of the low-concentration junction regions 39-1 and 39-2 and the high-concentration junction regions 44-1 and 44-2.

When the impurity ions are implanted for forming the high-concentration source and drain regions 44-1 and 44-2, high-concentration impurity ions are implanted into the semiconductor layer 33 through the silicide layers 43-1 and 43-2, so that the semiconductor layer 33 is protected by the silicide layers 43-1 and 43-2, thereby minimizing damage of the semiconductor layer 33 due to the ion implantation.

FIGS. 3K and 3L illustrate processes for forming source and drain electrodes,

which include depositing a metal material for the source and drain electrodes on the entire surface of the substrate. Subsequently, although not shown in the Figures, a third mask for forming the source and drain electrodes is used to pattern the silicide layers 43-1 and 43-2 so that the exposed silicide layers 43-1 and 43-2 are in direct contact with source and drain electrodes 46-1 and 46-2 having non-contact holes. Accordingly, the TFT according to embodiments of the present invention is fabricated.

According to the method of fabricating the TFT of the present invention as described above, only three masks composed of the first mask for forming the semiconductor layer 33, the second mask for forming the gate 37, and the third mask for forming the source and drain electrodes 46-1 and 46-2 are used, so that the process can be more simplified than the conventional method of fabricating the TFT using four masks.

That is, according to the method of fabricating the TFT of the present invention, the spacers 41 are formed on sidewalls of the gate 37, and the spacers 41 are used as masks to form the source and drain regions of LDD structure in the self-alignment manner, so that the conventional anodizing process is not required.

In addition, when the spacer 41 is formed, the gate insulating layer 34 below the spacer 41 is also etched to expose the high-concentration source and drain regions 46-1 and 46-2, so that the subsequent source and drain electrodes 46-1 and 46-2 are in direct contact with the source and drain regions 46-1 and 46-2 and electrically connected to each other. Accordingly, the conventional contact hole process for electrically connecting the source and drain electrodes to the source and drain regions is not required, so that one mask is reduced.

Further, according to the present invention, the gate capping layer 38 is

formed above the gate 37, and the spacers 41 are formed on their sidewalls to separate the gate 37 from the source and drain electrodes 46-1 and 46-2. Therefore, even when an interlayer insulating layer is formed and then the source and drain regions are not in contact with the source and drain electrodes through a contact hole in accordance with the conventional art, insulation between the gate 37 and the source and drain electrodes 46-1 and 46-2 can be sufficiently ensured.

According to the method of fabricating the TFT of the present invention, the silicide layers 43-1 and 43-2 are formed in the high-concentration source and drain regions 44-1 and 44-2, so that the silicide layers act as not only ion implantation barriers at the time of ion implantation for forming the high-concentration source and drain regions 44-1 and 44-2 but also etching barriers at the time of patterning the metal layer 45 for forming the source and drain electrodes 46-1 and 46-2, thereby enhancing an etch selectivity. The silicide layers 43-1 and 43-2 are formed between the high-concentration source and drain regions 44-1 and 44-2 and the source and drain electrodes 46-1 and 46-2, thereby reducing the contact resistance to enhance the device characteristics.

In addition, the method of fabricating the TFT of the present invention prevents impurity ions from flowing into the gate 37 by means of the gate capping layer 38 when the ions are implanted for forming the low-concentration source and drain regions 39-1 and 39-2, thereby enhancing the device characteristics.

Embodiments illustrated in FIGS. 3A to 3L are related to a method of fabricating the TFT having the LDD structure, however, after the gate is formed, when the spacers 41 are formed and then high-concentration impurity ions are implanted without the process of implanting low-concentration impurity ions of FIG.

3E, the TFT having an offset structure can be fabricated.

FIG. 4 illustrates a circuit diagram of an organic EL display device in accordance with embodiments of the present invention.

The organic EL display device according to the embodiments of the present invention is composed of a transparent insulating substrate 100 allowing light to be transmitted, a signal line 150 formed on the substrate 100, and pixels 160 connected to the signal line and arranged in a matrix.

The signal line 150 includes a plurality of data lines 130, a plurality of power supply lines 140, and a plurality of gate lines 120.

The data lines 130 acts to apply a data voltage to the pixels 160, and are spaced apart from each other by a predetermined interval. The power supply lines 140 are adjacent to the respective data lines 130 and are arranged parallel to the respective data lines 130, and act to always supply power to the pixels 160 while the organic EL display device 100 operates. The gates 140 cross the data lines 130 and the power supply lines 140 and are spaced apart from each other by a predetermined interval, and act to apply signals for turning on/off the TFTs of the pixels 160.

The pixels 160 are arranged at locations where the respective data lines 130 and the respective gate lines 120 cross each other in a matrix, and each of the pixels 160 is composed of two TFTs 170 and 200, a charge capacitor 180, and an organic EL diode 300 as shown in FIG. 2.

The first TFT 170 of the two TFT 170 and 200 is connected to a corresponding gate line among the gate lines 120, and is driven by a signal applied through the gate line. The capacitor connected between the first TFT 170 and a

corresponding power supply line among the power supply lines 140 is a charge capacitor for maintaining data applied from the corresponding data line among the data lines 130 so as to have the organic EL display device 100 keep the image during one frame.

The second TFT 200 is connected to the first TFT 170 and the capacitor 180, and acts to drive the organic EL diode 300.

FIG. 5 illustrates one pixel 160 of the organic EL display device 100 shown in FIG. 4, that is, illustrates the layout of the location denoted by A of FIG. 4.

Referring to FIG. 5 with the planar structure of the organic EL display device according to embodiments of the present invention, a corresponding gate line 120 among the gate lines is arranged across a corresponding data line 130 among the data lines arranged parallel to each other, and a corresponding power supply line 140 among the power supply lines.

The first TFT 170 and the capacitor 180 are disposed in an upper portion of the pixel region defined by the data line 130, the gate line 120, and the power supply line 140, and the second TFT 200 and the organic EL diode 300 are disposed in a lower portion.

The first TFT 170 connected to the gate line 120 and the data line 130 has its gate 174 extending from the gate line 120, the semiconductor layer 172 is formed below the gate 174, and the source electrode 176 and the drain electrode 178 extending from the data line 130 are in direct contact with the semiconductor layer 172 where the high-concentration source and drain regions are formed without contact holes.

The drain electrode 178 of the first TFT 170 is connected to a first electrode

182 of the capacitor 180 through a connection pad 315, and a second electrode 184 extending from the power supply line 140 is arranged on the first electrode 182.

The drain electrode 178 is connected to the connection pad 315 through a contact hole 261, and the first electrode 182 of the capacitor 180 is connected to the connection pad 315 through the contact hole 262, so that the first TFT 170 and the capacitor 180 are electrically connected to each other.

In this case, the first electrode 182 of the capacitor 180 is formed of the same material as the gate line 120 and the gate 174, so that it is simultaneously formed when the gate line 120 and the gate 174 are formed. The second electrode 184 of the capacitor 180 is formed of the same material as the data line 130, the source and drain electrodes 176 and 178, and the power supply line 140, so that it is simultaneously formed when the data line 130, the source and drain electrodes 176 and 178, and the power supply line 140 are formed.

In the meantime, the second TFT 200 connected to the capacitor 180 and the power supply line 140 has a gate 220 extending from the first electrode 182 of the capacitor 180 and formed on the semiconductor layer 210, and a source electrode 250 and a drain electrode 255 of the capacitor which extend from the power supply line 140 are in direct contact with each other without contact holes in the semiconductor layer 210 where the high-concentration source and drain regions are formed.

The drain electrode 255 of the second TFT 200 is in contact with an anode electrode 310 of the organic EL diode 300 as a transparent electrode through a contact hole 267, and the second TFT 200 is electrically connected to the organic EL diode 300.

The method of fabricating the organic EL display device of the present invention having the above-described structure uses the method of fabricating the TFT shown in FIGS. 3A to 3L, and descriptions thereof will be given with reference to FIGS. 6A to 6Q and FIGS. 7 to 9 below.

FIGS. 6A to 6Q are cross-sectional views taken along line 5A-5A' of FIG. 5, which explains the process of fabricating the second TFT 200 and the organic EL diode 300. FIG. 9 is a cross-sectional view taken along line 5B-5B' of FIG. 5, which illustrates a cross-sectional view illustrating the method of fabricating the first TFT 170 and the capacitor 180.

FIGS. 6A and 6B illustrate processes for forming a semiconductor layer on a substrate, which includes forming a SiO_2 layer 202 on the transparent insulating substrate 100 as a buffer layer, and forming a polysilicon layer 210a thereon.

Subsequently, the polysilicon layer 210a is patterned using a first mask (not shown) for forming a semiconductor layer. Accordingly, a semiconductor layer 210 of the second TFT 200 is formed on the buffer layer 202.

In this case, the semiconductor layer 172 of the first TFT 170 is also formed when the semiconductor layer 210 of the second TFT 200 is formed as shown in FIG. 9.

FIGS. 6C and 6D illustrate processes for forming a gate, which include sequentially forming a gate insulating layer 215, a gate electrode material 220a, and a gate capping material 225a on the buffer layer 202 having the semiconductor layer 172 of the first TFT 170 (see FIG. 9) and the semiconductor layer 210 of the second TFT 200.

Subsequently, although not shown in the Figures, the gate capping material

225a and the gate electrode material 220a are sequentially etched using a second mask for forming a gate to form a gate 220 of the second TFT 200 and a gate capping layer 225. In addition, a lower electrode as the first electrode 182 of the first capacitor 180 and a dielectric layer 183 are simultaneously formed while the gate 174 of the first TFT 170 and the gate capping layer 225 are formed as shown in FIG. 9. In this case, a nitride layer or an oxide layer is employed as the gate capping layer 225 of the first and second TFTs 170 and 200 and the dielectric layer 183 of the first capacitor 180.

In this case, when the gates 174 and 220 of the first and second TFTs 170 and 200 are formed, although not shown in the Figure, the gate line 130 is also simultaneously formed.

FIG. 6E illustrates a process for forming low-concentration source and drain regions, which implants low-concentration impurity ions having a predetermined conductivity type, e.g., p-type or n-type low-concentration impurity ions into the semiconductor layer 210 of the second TFT 200 using the gate 220 as a mask. Accordingly, low-concentration source and drain regions 214 are formed in the semiconductor layer 210 at both sides of the gate 220.

The low-concentration impurity ions are simultaneously implanted into the semiconductor layer 172 using the gate 174 of the first TFT 170 as a mask to form low-concentration source and drain regions 173 of the first TFT 170.

In this case, a gate capping layer 225 is formed on each of the gates 172 and 220 of the first and second TFTs 170 and 200, and the dielectric layer 183 is also formed on the first electrode 182 of the capacitor 180, thereby acting as an ion implantation barrier at the time of implanting the lower concentration impurity ions.

The semiconductor layer 212 between the low-concentration source and drain regions 214 in the semiconductor layer 210 of the second TFT 200, and the semiconductor layer 172 between the low-concentration source and drain regions 173 of the first TFT 170 act as channel regions.

FIGS. 6F and 6G illustrate processes for forming spacers on sidewalls of the gate 220. A spacer insulating layer 230a, e.g., an SiO_2 layer or an SiNx layer is first deposited on the gate insulating layer 215 having the gate 220 of the second TFT 200, and then etched-back to form spacers 230 on the sidewall of the gate 220.

In this case, referring to FIG. 9, the spacers 230 are simultaneously formed on sidewalls of the first electrode 182 of the capacitor 200 and the gate 174 of the first TFT 170.

When the insulating layer 230a for forming the spacers 230 is etched, the gate insulating layer 215 below the insulating layer 230a is also etched to expose the low-concentration source and drain regions 173 and 214 of the first and second TFTs 170 and 200.

FIGS. 6H and 6I are processes for forming a silicide layer on the exposed low-concentration source and drain regions 214, which include first depositing a high melting point metal layer 240a on the entire surface of the substrate, and annealing the metal layer at a temperature of 500°C or lower, so that a silicide layer 240 is formed on the exposed low-concentration source and drain regions 214 of the semiconductor layer 210 while the metal layer 240a still remains in the rest of regions.

Accordingly, when the remaining metal layer 240a is removed, the silicide layer 240 is formed only in the exposed low-concentration source and drain regions

214.

The silicide layer 240 is also formed on the exposed low-concentration source and drain regions 173 of the first TFT 170 as shown in FIG. 9.

FIG. 6J illustrates a process for forming high-concentration source and drain regions, which includes implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions 214 into the semiconductor layer using the spacers 240 and the gate 220 of the second TFT 200 as masks to form high-concentration source and drain regions 216 in the semiconductor layer below the silicide layer 240 in a self-alignment manner.

In this case, the high-concentration source and drain regions 175 are formed also below the silicide layer 240 of the first TFT 170 as shown in FIG. 9.

Accordingly, the source and drain regions of the first and second TFTs 170 and 200 have an LDD structure composed of the low-concentration junction regions 173 and 175 and the high-concentration junction regions 214 and 216.

At the time of implanting ions for forming the high-concentration source and drain regions 175 and 216, the silicide layer 240 acts as an ion implantation barrier of the semiconductor layers 172 and 210, so that the damage of the semiconductor layers 172 and 210 can be minimized.

FIGS. 6K and 6L illustrate process for forming source and drain electrodes, which include depositing a metal material for source and drain electrodes 250a on the entire surface of the substrate, and although not shown in the Figures, forming source and drain electrodes 250 and 255 of the second TFT 200 in direct contact with the silicide layer 240 that is patterned and exposed using a third mask for forming the source and drain electrodes without contact holes.

The source and drain electrodes 176 and 178 of the first TFT 170 are in direct contact with the silicide layer 240. Although not shown in the Figures, when the source and drain electrodes 176, 178, 250, and 255 of the first and second TFTs 170 and 200 are formed, the data line 130 and the power supply line 140 are simultaneously formed.

Accordingly, the TFTs 170 and 200 of the organic EL display device of the present invention are fabricated.

FIGS. 6M and 6P illustrate processes for forming an anode electrode of an organic EL diode, which include forming a planarization layer 260 as an interlayer insulating layer on the entire surface of the substrate, and etching the planarization layer 260 to form a contact hole 267 using a fourth mask for forming the contact hole, although not shown in the Figures, such that the drain electrode 255 of the second TFT 200 is exposed.

Subsequently, after a transparent conductive layer 310a is deposited on the planarization layer 260 having the contact hole 267, although not shown in the Figures, the transparent conductive layer 310a is patterned using a fifth mask for forming an anode electrode to from a pixel electrode 310. In this case, the pixel electrode 310 acts as an anode electrode 310 of the organic EL diode 300. An Indium Tin Oxide (ITO) layer or an Indium Zinc Oxide (IZO) layer is employed as the transparent conductive layer 310a.

In addition, as shown in FIG. 9, when the planarization layer 260 is etched using the fourth mask to form a contact hole 267, contact holes 261 and 262 are formed so as to expose the drain electrode 178 of the first TFT 170 and the first electrode 182 of the capacitor 180, and a connection pad 315 formed of a

transparent conductive layer is simultaneously formed to connect the drain electrode 178 of the first TFT 170 to the first electrode 182 of the capacitor 180 via the contact holes 261 and 262.

Instead of the method of forming the contact hole 267 so as to expose the drain electrode 255 of the second TFT 200 and the buffer layer 202 as shown in FIG. 6N as the method of forming the contact hole 267 for forming the anode electrode 310 of the organic EL diode 300, contact holes 267 and 267a for respectively exposing the drain electrode 267 and the buffer layer 202 may be formed as shown in FIG. 7, respectively, or the contact hole 267 for exposing only the drain electrode 255 may be formed as shown in FIG. 8.

FIG. 6Q illustrates a process for forming a cathode electrode 330 and an organic thin layer 320 of the organic EL diode 300, which sequentially forms the organic thin layer 320 and the cathode layer 330 on the planarization layer 260 having the anode electrode 310. In this case, the organic thin layer 320 and the cathode electrode 330 are not formed in a portion where the first TFT 170 and the capacitor 180 are formed as shown in FIG. 9. In this case, the cathode electrode 330 is formed of a metal layer having a smaller work function than the anode electrode 310.

Although not shown in the Figure, the organic thin layer 320 is composed of a hole transport layer, an emission layer, and an electron transport layer. In this case, the hole transport layer transports holes injected from the anode electrode 310 to the emission layer, the electron transport layer transports electrons injected from the cathode electrode 330 to the emission layer, and the transported holes and electrons are recombined in the emission layer to emit light. That is, when the

holes and electrons are recombined, organic molecules constituting the emission layer are excited to create excitons, and the excitons are inactivated to cause light to be emitted from the emission layer.

The method of fabricating the organic EL display device according to the present invention has been described the case of using the TFT having an LDD structure as a switching device, however, when the process of forming the low-concentration source and drain ions of FIG. 6E is omitted after the gate 220 of the second TFT 200 is formed in FIG. 6D, the high-concentration source and drain regions 214 are spaced apart from the gate 220 by a predetermined interval so that the TFT having an offset structure can be fabricated. This is also the same in the case of the first TFT 170.

According to the method of fabricating the organic EL display device of embodiments of the present invention as described above, only five masks composed of three masks for forming TFT and two masks for forming an organic EL diode are used, so that two masks can be reduced compared to the conventional method of fabricating the organic EL display device using seven masks. In addition, the source and drain regions are formed in a self-alignment manner using spacers without anodization, so that the process is simplified.

[Effect of the Invention]

According to a method of fabricating a TFT and an organic EL display device of the present invention as described above, source and drain regions are made to be in direct contact with source and drain electrodes, so that the number of masks can be reduced to simplify a process , thereby reducing the fabrication cost thereof.

In addition, the source and drain regions are formed in a self-alignment

method using a spacer without anodization, so that the process can be simplified and the fabrication cost can be reduced.

Further, a silicide layer can be formed between the source and drain regions and the source and drain electrodes to reduce contact resistance. In addition, the silicide layer can act as not only an etching barrier to enhance an etch selectivity at the time of forming the source and drain electrodes but also a barrier at the time of implanting ions for forming the source and drain regions to minimize damage of a semiconductor layer.

Additionally, a gate capping layer is formed on a gate at the time of implanting the ions for forming low-concentration source and drain regions to act as a barrier with respect to the ion implantation, so that the gate can be protected.

The present invention has been described with an organic electroluminescence display as an example, however, the present invention is not limited thereto but may be applied to a display device such as a liquid crystal display device using a TFT as a switching device.

[Scope of the Claim]

[Claim 1] A method of fabricating a thin film transistor (TFT), comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

implanting high-concentration impurity ions into the exposed semiconductor layer and forming high-concentration source and drain regions; and

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

[Claim 2] The method according to claim 1, wherein forming the spacer comprising:

forming an insulating layer on the gate insulating layer including the gate; and

etching the insulating layer and the gate insulating layer to form the spacer on the sidewall of the gate and simultaneously exposing the semiconductor layer.

[Claim 3] The method according to claim 2, wherein one of an oxide layer and a nitride layer is used as the insulating layer for the spacer.

[Claim 4] The method according to claim 1, wherein the high-concentration source and drain regions have an offset structure that is spaced apart from the gate by a predetermined interval and formed in the semiconductor layer.

[Claim 5] The method according to claim 1, further comprising:

between forming the gate and forming the spacer,

forming a lightly doped drain (LDD) structure by implanting low-concentration impurity ions having the same conductivity as the high-concentration source and drain regions into the semiconductor layer using the gate as a mask and forming low-concentration source and drain regions.

[Claim 6] The method according to claim 5, wherein the gate capping layer acts as an ion implantation barrier of the gate at the time of implanting the ions for forming the low-concentration source and drain regions.

[Claim 7] The method according to claim 6, wherein one of an oxide layer and a nitride layer is used as the gate capping layer.

[Claim 8] The method according to claim 1, further comprising:

between forming the spacer and forming the high-concentration source and drain regions,

forming a silicide layer on the exposed semiconductor layer.

[Claim 9] The method according to claim 8, wherein the silicide layer acts as an ion implantation barrier of the semiconductor layer at the time of implanting the ions for forming the high-concentration source and drain regions.

[Claim 10] The method according to claim 8, wherein the silicide layer acts as an etching barrier against a metal layer at the time of depositing and patterning the metal layer on the substrate to form the source and drain electrodes.

[Claim 11] An active matrix display device fabricated by the method of fabricating the thin film transistor (TFT) according to claim 1.

[Claim 12] A method of fabricating a thin film transistor (TFT), comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

forming a silicide layer on the exposed semiconductor layer;

implanting high-concentration impurity ions into the semiconductor layer below the silicide layer, and forming high-concentration source and drain regions having an offset structure spaced apart from the gate by a predetermined interval; and

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

[Claim 13] The method according to claim 12, wherein forming the spacer comprising:

forming an insulating layer on the gate insulating layer including the gate; and

etching the insulating layer and the gate insulating layer to form the spacer on the sidewall of the gate and simultaneously exposing the semiconductor layer.

[Claim 14] The method according to claim 13, wherein one of an oxide layer and a nitride layer is used as the insulating layer for the spacer.

[Claim 15] The method according to claim 12, wherein one of an oxide layer and a nitride layer is used as the gate capping layer.

[Claim 16] The method according to claim 12, wherein the silicide layer acts as an ion implantation barrier of the semiconductor layer at the time of implanting the ions for forming the high-concentration source and drain regions.

[Claim 17] The method according to claim 12, wherein the silicide layer acts as an etching barrier against a metal layer at the time of depositing and patterning the metal layer on the substrate to form the source and drain electrodes.

[Claim 18] The method according to claim 12, wherein the high-concentration impurity ions are n- or p-type impurity ions.

[Claim 19] An active matrix display device fabricated by the method of fabricating the thin film transistor (TFT) according to claim 12.

[Claim 20] A method of fabricating a thin film transistor (TFT), comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask to form low-concentration source and drain regions;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

forming a silicide layer on the exposed semiconductor layer;

forming a lightly doped drain (LDD) structure by implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the semiconductor layer below the silicide layer and forming high-concentration source and drain regions; and

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask.

[Claim 21] The method according to claim 20, wherein forming the spacer comprising:

forming an insulating layer on the gate insulating layer including the gate; and

etching the insulating layer and the gate insulating layer to form the spacer on the sidewall of the gate and simultaneously exposing the semiconductor layer.

[Claim 22] The method according to claim 21, wherein one of an oxide layer and a nitride layer is used as the insulating layer for the spacer.

[Claim 23] The method according to claim 20, wherein the gate capping layer acts as an ion implantation barrier of the gate at the time of implanting the ions for forming the low-concentration source and drain regions.

[Claim 24] The method according to claim 23, wherein one of an oxide layer and a nitride layer is used as the gate capping layer.

[Claim 25] The method according to claim 20, wherein the silicide layer acts as an ion implantation barrier of the semiconductor layer at the time of implanting the ions for forming the high-concentration source and drain regions.

[Claim 26] The method according to claim 20, wherein the silicide layer acts as an etching barrier against a metal layer at the time of depositing and patterning the metal layer on the substrate to form the source and drain electrodes.

[Claim 27] The method according to claim 20, wherein the high-concentration impurity ions are n- or p-type impurity ions.

[Claim 28] An active matrix display device fabricated by the method of fabricating the thin film transistor (TFT) according to claim 20.

[Claim 29] A thin film transistor (TFT), comprising:

a semiconductor layer disposed on an insulating substrate;

a gate insulating layer disposed on the semiconductor layer to expose both sides of the semiconductor layer;

a gate disposed on the gate insulating layer;

a gate capping layer disposed on the gate;

a spacer disposed on sidewalls of the gate capping layer and the gate on the gate insulating layer;

high-concentration source and drain regions disposed in the exposed semiconductor layer; and

source and drain electrodes in direct contact with the high-concentration source and drain regions.

[Claim 30] The TFT according to claim 29, wherein the high-concentration source and drain regions have an offset structure that is spaced apart from the gate by a predetermined interval and disposed in the semiconductor layer.

[Claim 31] The TFT according to claim 29, further comprising:

a lightly doped drain (LDD) structure including low-concentration source and drain regions having the same conductivity as the high-concentration source and drain regions and disposed in the semiconductor layer between the gate and the high-concentration source and drain regions below the spacer.

[Claim 32] The TFT according to claim 29, wherein the high-concentration impurity ions are n- or p-type impurity ions.

[Claim 33] The TFT according to claim 29, wherein the gate capping layer and the spacer are formed of one of an oxide layer and a nitride layer.

[Claim 34] The TFT according to claim 29, further comprising:

a silicide layer disposed between the source and drain regions and the source and drain electrodes.

[Claim 35] A method of fabricating an active matrix display device, comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

forming a spacer on a sidewall of the gate and simultaneously exposing the

semiconductor layer;

implanting high-concentration impurity ions into the exposed semiconductor layer, and forming high-concentration source and drain regions having an offset structure spaced apart from the gate by a predetermined interval;

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask;

forming a planarization layer on the entire surface of the substrate;

etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole; and

forming a pixel electrode on an interlayer insulating layer including the contact hole using a fifth mask.

[Claim 36] The method according to claim 35, further comprising:

between forming the spacer and forming the high-concentration source and drain regions,

forming a silicide layer on the exposed semiconductor layer.

[Claim 37] The method according to claim 35, wherein the high-concentration impurity ions are n- or p-type impurity ions.

[Claim 38] An active matrix display device fabricated by the method of fabricating the active matrix display device according to claim 35.

[Claim 39] A method of fabricating an active matrix display device,

comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask and forming low-concentration source and drain regions;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

forming a lightly doped drain (LDD) structure by implanting high-concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the exposed semiconductor layer and forming high-concentration source and drain regions;

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask;

forming a planarization layer on the entire surface of the substrate;

etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole; and

forming a pixel electrode on an interlayer insulating layer including the contact hole using a fifth mask.

[Claim 40] The method according to claim 39, further comprising:

between forming the spacer and forming the high-concentration source and

drain regions,

forming a silicide layer on the exposed semiconductor layer.

[Claim 41] The method according to claim 39, wherein the high-concentration impurity ions are n- or p-type impurity ions.

[Claim 42] An active matrix display device fabricated by the method of fabricating the active matrix display device according to claim 39.

[Claim 43] A method of fabricating an active matrix display device, comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate having a gate capping layer on the gate insulating layer using a second mask;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

forming a silicide layer on the exposed semiconductor layer;

Implanting high-concentration impurity ions into the semiconductor layer below the silicide layer to form high-concentration source and drain regions having an offset structure that is spaced apart from the gate by a predetermined interval;

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask;

forming a planarization layer on the entire surface of the substrate;

etching the planarization layer and exposing one of the source and drain electrodes using a fourth mask to form a contact hole;

forming an anode electrode on an interlayer insulating layer including the contact hole using a fifth mask;

forming an organic thin layer on the anode electrode; and

forming a cathode electrode on the organic thin layer.

[Claim 44] An active matrix display device fabricated by the method of fabricating the active matrix display device according to claim 43.

[Claim 45] A method of fabricating an active matrix display device, comprising:

forming a semiconductor layer on an insulating substrate using a first mask;

forming a gate insulating layer on the insulating substrate including the semiconductor layer;

forming a gate and a gate capping layer on top of the gate on the gate insulating layer on the semiconductor layer using a second mask;

implanting low-concentration impurity ions into the semiconductor layer using the gate as a mask and forming low-concentration source and drain regions;

forming a spacer on a sidewall of the gate and simultaneously exposing the semiconductor layer;

forming a silicide layer on the exposed semiconductor layer;

forming a lightly doped drain (LDD) structure by implanting high-

concentration impurity ions having the same conductivity as the low-concentration source and drain regions into the semiconductor layer below the silicide layer and forming high-concentration source and drain regions;

forming source and drain electrodes in direct contact with the high-concentration source and drain regions using a third mask;

forming a planarization layer on an entire surface of the substrate;

etching the planarization layer and exposing any one of the source and drain electrodes using a fourth mask to form a contact hole;

forming an anode electrode on an intermediate insulating layer including the contact hole using a fifth mask;

forming an organic thin layer on the anode electrode; and

forming a cathode electrode on the organic thin layer.

[Claim 46] An active matrix display device fabricated by the method of fabricating the active matrix display device according to claim 45.

[Claim 47] An active matrix display device, comprising:

a gate line and a data line crossing each other and arranged on an insulating substrate;

a power supply line crossing the gate line and arranged parallel to the data line; and

a pixel disposed in a pixel region defined by the gate line, the data line, and the power supply line,

the pixel including:

a first thin film transistor (TFT) having a first gate, a first semiconductor layer, and first source and drain electrodes;

a second TFT having a second gate, a second semiconductor layer, and second source and drain electrodes;

a capacitor having first and second electrodes; and

a pixel electrode,

wherein the first source and drain electrodes of the first TFT are in direct contact with the first semiconductor layer, one of the first source and drain electrodes is connected to the first electrode of the capacitor through a connection pad, the second source and drain electrodes of the second TFT are in direct contact with the second semiconductor layer, and one of the second source and drain electrodes is in contact with the pixel electrode through a contact hole.

[Claim 48] The active matrix display device according to claim 47, wherein the first gate of the first TFT extends from the gate line, the second gate of the second TFT extends from the first electrode of the first capacitor, the second electrode of the second capacitor extends from the power supply line, the other of the second source and drain electrodes of the second TFT extends from the power supply line, and the other of the source and drain electrodes of the first TFT extends from the data line.

[Claim 49] An active matrix display device comprising a gate line and a data line crossing each other and arranged on an insulating substrate, a power supply line crossing the gate line and arranged parallel to the data line, and a pixel

disposed in a pixel region defined by the gate line, the data line and the power supply line and having first and second thin film transistors (TFT), a capacitor, and a pixel electrode, the active matrix display device comprising:

a first semiconductor layer of the first TFT and a second semiconductor layer of the second TFT disposed on the insulating substrate;

first and second gate insulating layers disposed on the first and second semiconductor layers to expose both sides of the respective first and second semiconductor layers, and a third gate insulating layer disposed on the substrate;

first and second gates of the first and second TFTs, the first and second gates having first and second capping layers thereon and disposed on the first and second gate insulating layers, respectively;

a first electrode of the capacitor having a dielectric layer thereon and disposed on the third gate insulating layer;

a spacer disposed on sidewalls of the first electrode of the capacitor and the first and second gates of the first and second TFTs;

a high-concentration source region of the first TFT disposed in the exposed first semiconductor layer and a high-concentration source region of the second TFT disposed in the exposed second semiconductor layer;

first and second source and drain electrodes of the first and second TFTs respectively disposed on the substrate and in direct contact with the first and second source and drain regions;

a second electrode of the capacitor disposed on the dielectric layer of the capacitor;

a planarization layer having first and second contact holes exposing

respective ones of the first and second source and drain electrodes of the respective first and second TFTs, and a third contact hole exposing the first electrode of the capacitor;

a pixel electrode connected to one of the second source and drain electrodes of the second TFT through the first contact hole on the planarization layer; and

a connection pad disposed to connect one of the first source and drain electrodes of the first TFT to the first electrode of the first capacitor through the respective second and third contact holes on the planarization layer.

[Claim 50] The active matrix display device according to claim 49, wherein the first and second high-concentration source and drain regions have an offset structure spaced apart from the first and second gates by predetermined intervals, respectively.

[Claim 51] The active matrix display device according to claim 49, further comprising:

first and second low-concentration source and drain regions disposed below the spacer of the first and second TFTs, respectively,

wherein the first and second low-concentration source and drain regions and the first and second high-concentration source and drain regions form lightly doped drain (LDD) structures.

[Claim 52] The active matrix display device according to claim 49, wherein

the first and second high-concentration source and drain regions are n- or p-type impurity ions.

[Claim 53] A method of fabricating an active matrix display device comprising a gate line and a data line crossing each other and arranged on an insulating substrate, a power supply line crossing the gate line and arranged parallel to the data line, and a pixel formed in a pixel region defined by the gate line, the data line and the power supply line, the pixel having first and second thin film transistors (TFT), a capacitor, and a pixel electrode, the method comprising:

forming a first semiconductor layer of a first thin film transistor (TFT) and a second semiconductor layer of a second TFT on the substrate using a first mask;

forming a gate insulating layer on the substrate including the first and second semiconductor layers;

forming first and second gates including respective first and second gate capping layers on the gate insulating layer of the respective first and second semiconductor layers, a first electrode of the capacitor including a dielectric layer on the gate insulating layer, and the gate line using a second mask;

forming a spacer on a sidewall of the first electrode and sidewalls of the first and second gates and simultaneously exposing the first and second semiconductor layers;

forming first high-concentration source and drain regions of the first TFT in the exposed first semiconductor layer, and second high-concentration source and drain regions of the second TFT in the exposed second semiconductor layer;

forming first source and drain electrodes in direct contact with the first high-

concentration source and drain regions, second source and drain electrodes in direct contact with the second high-concentration source and drain regions, a second electrode of the capacitor on the dielectric layer, and the data line and the power supply line on the substrate using a third mask;

forming a planarization layer on the entire surface of the substrate;

etching the planarization layer and forming a first contact hole exposing one of the first high-concentration source and drain regions, a second contact hole exposing one of the second high-concentration source and drain regions, and a third contact hole exposing the first electrode of the capacitor using a fourth mask; and

forming a pixel electrode connected to one of the first high-concentration source and drain regions through the first contact hole, and a connection pad connecting one of the second high-concentration source and drain regions to the first electrode of the capacitor through the second and third contact holes using a fifth mask.

[Claim 54] An active matrix display device fabricated by the method of fabricating the active matrix display device according to claim 53.

FIG.1A

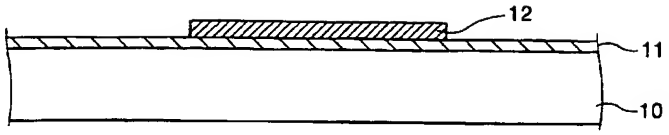


FIG.1B

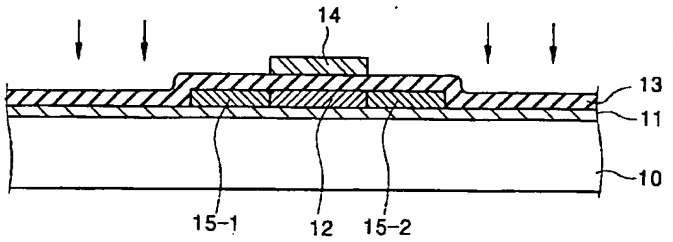


FIG.1C

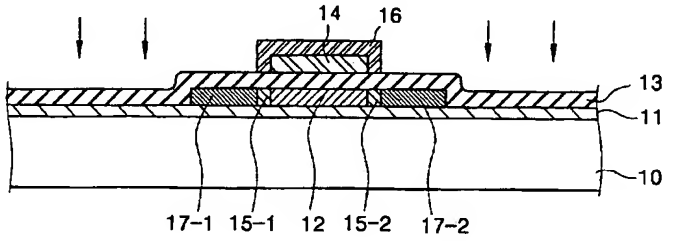


FIG.1D

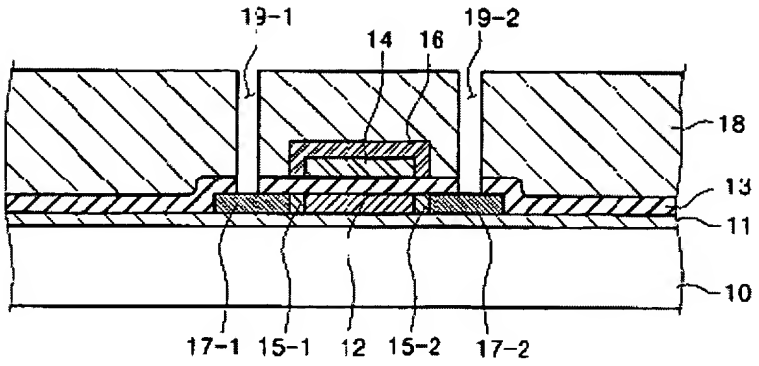


FIG.1E

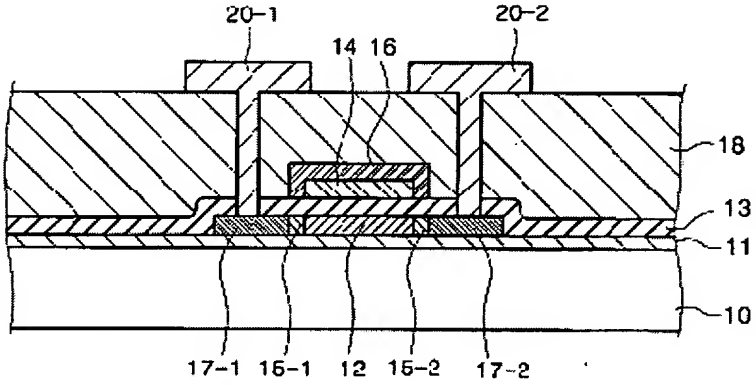


FIG.2A

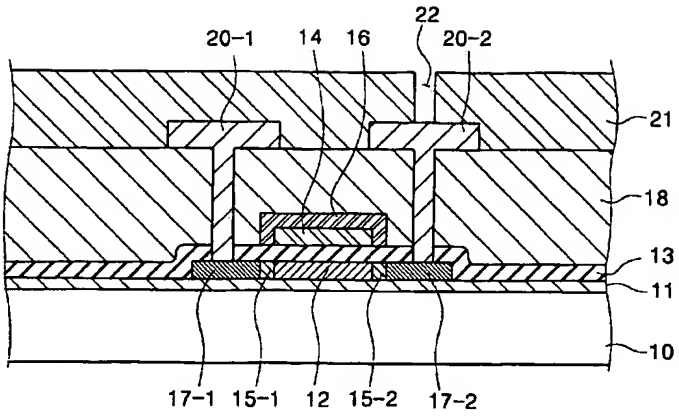


FIG.2B

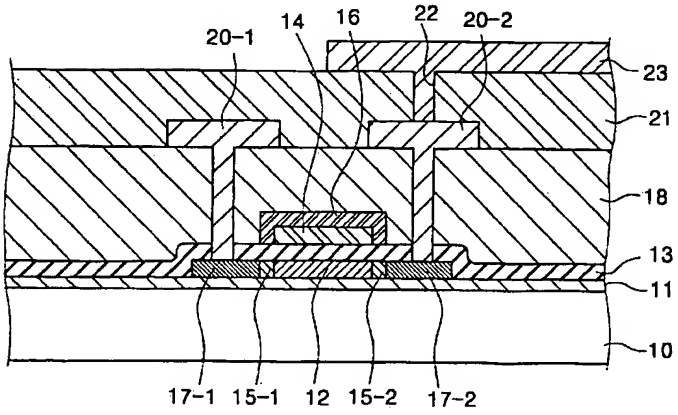


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FIG.2C

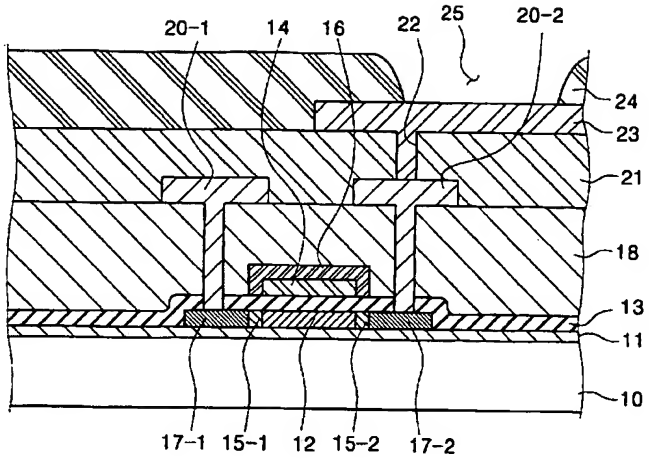
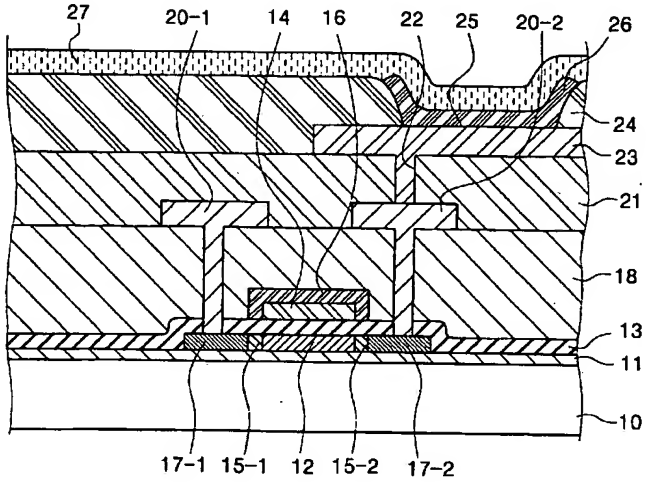


FIG.2D



5

FIG.3A

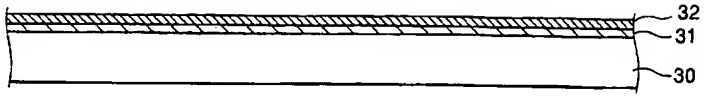


FIG.3B

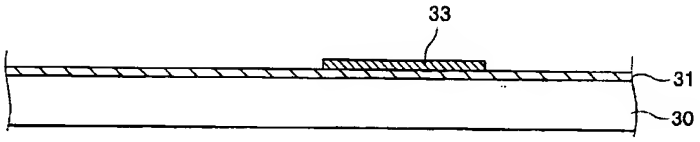


FIG.3C

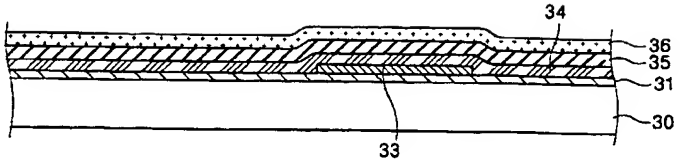


FIG.3D

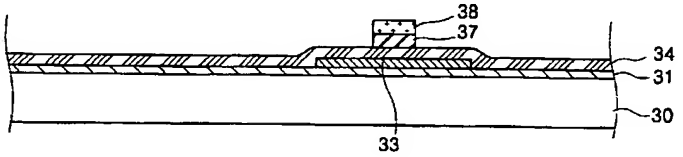


FIG.3E

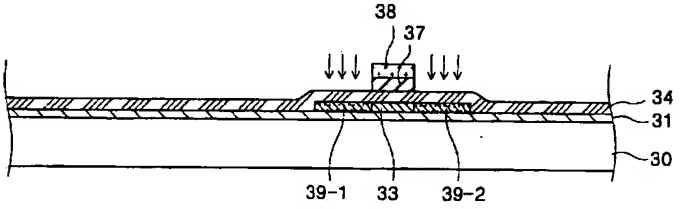


FIG.3F

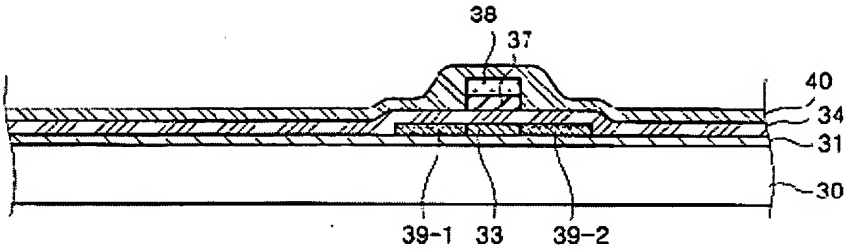


FIG.3G

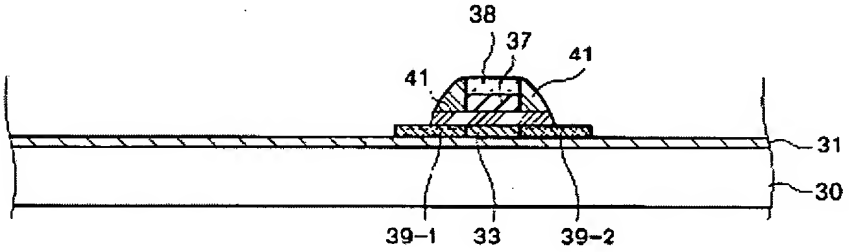


FIG.3H

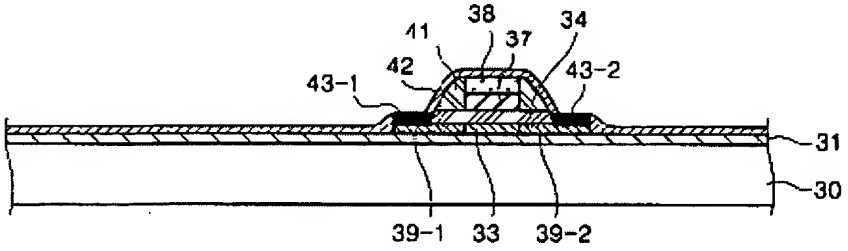


FIG.3I

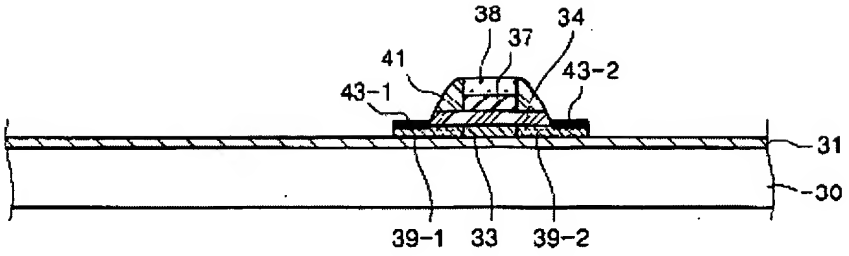


FIG.3J

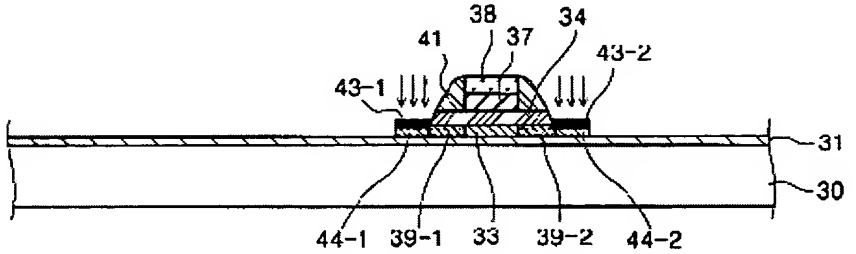


FIG.3K

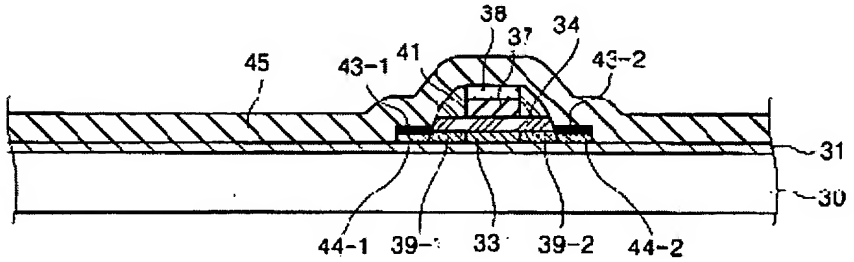


FIG.3L

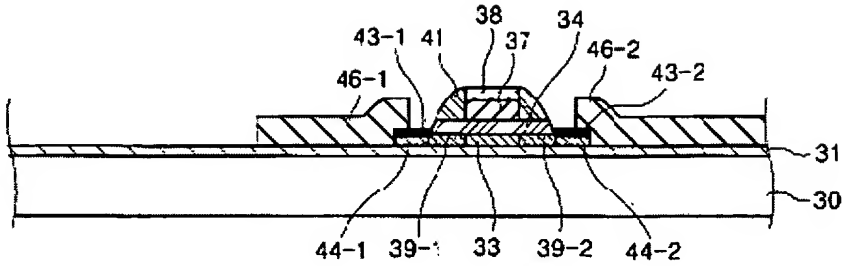


FIG.4

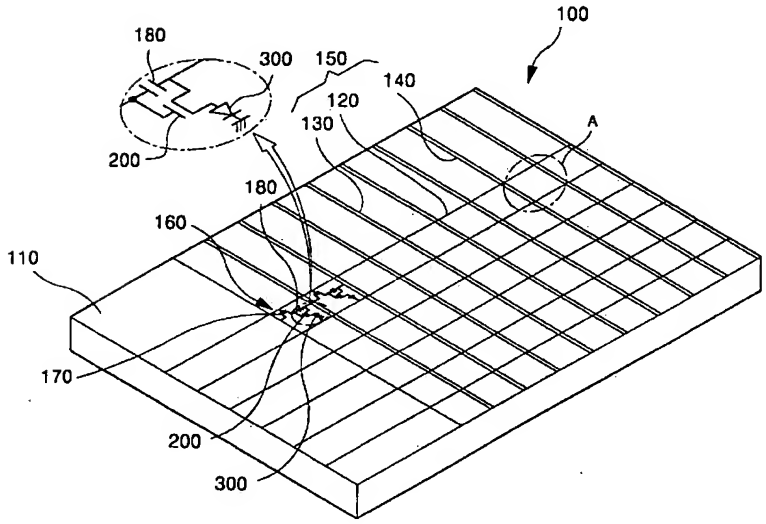


FIG.5

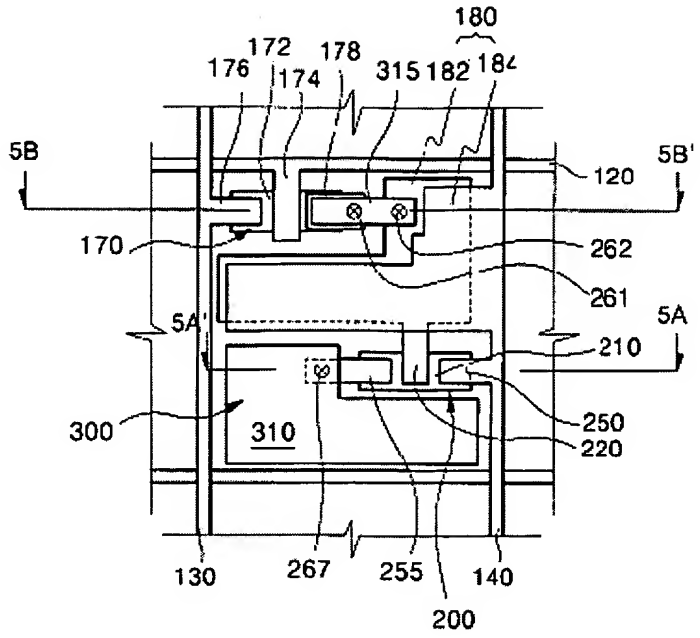
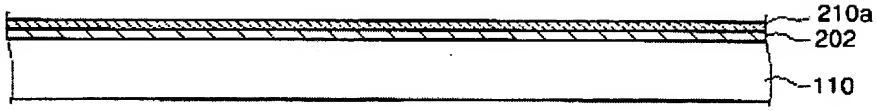


FIG.6A



5

FIG.6B

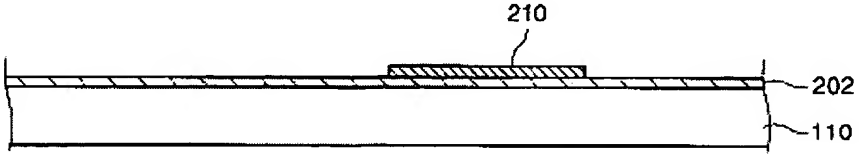


Fig.6C

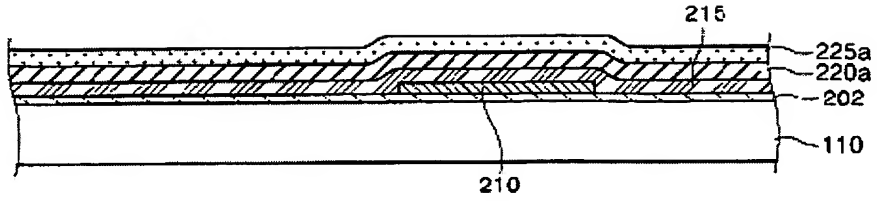


FIG.6D

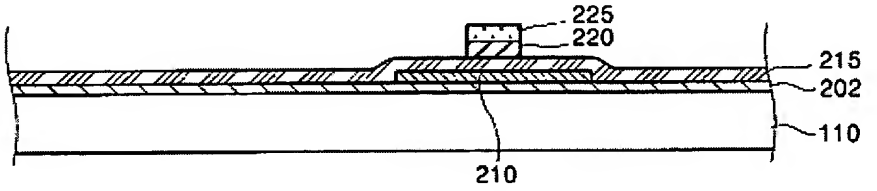


FIG.6E

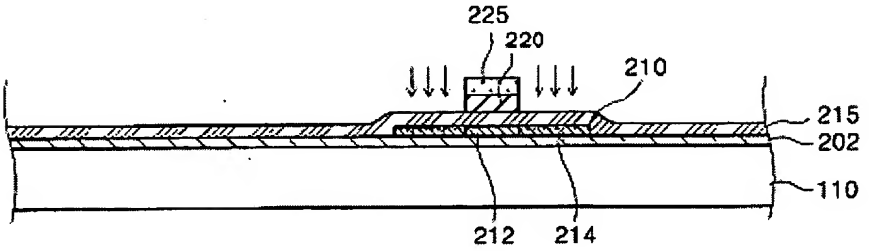


FIG.6F

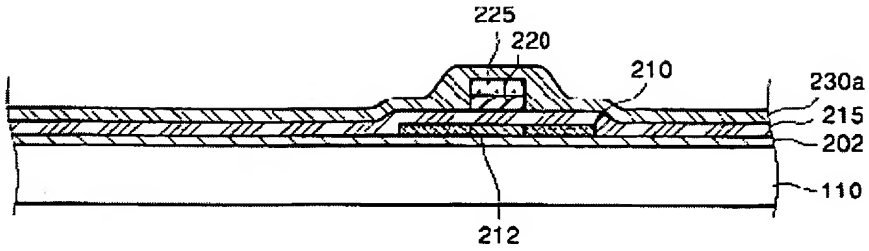


FIG.6G

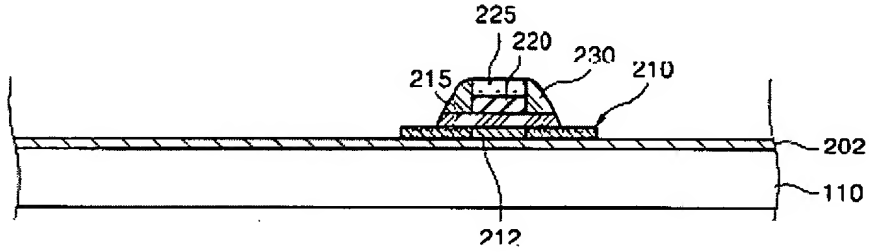


FIG.6H

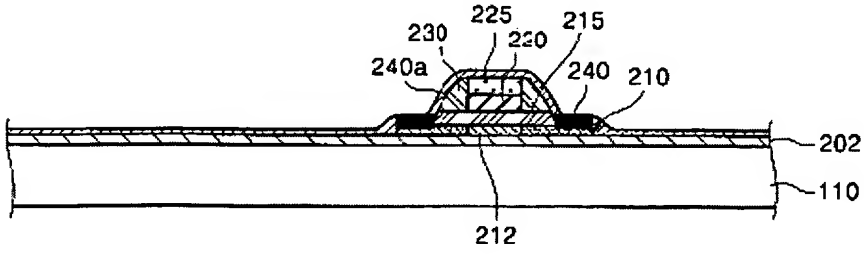


FIG.6I

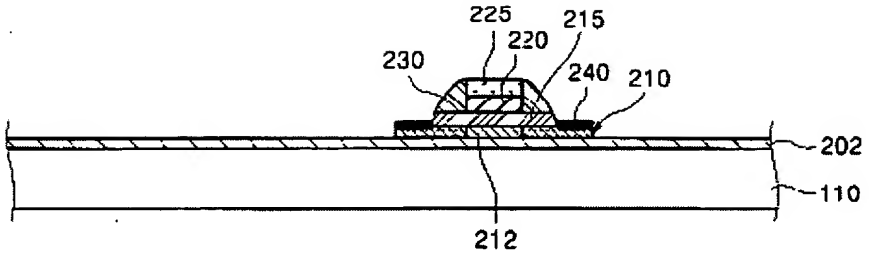


FIG.6J

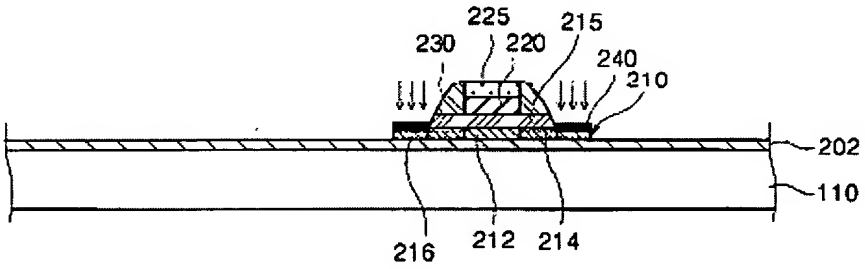


FIG.6K

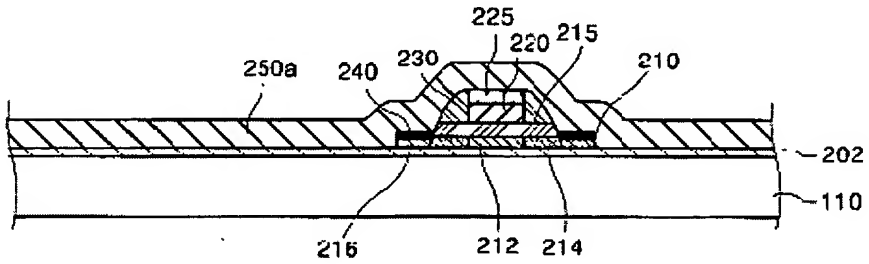


FIG.6L

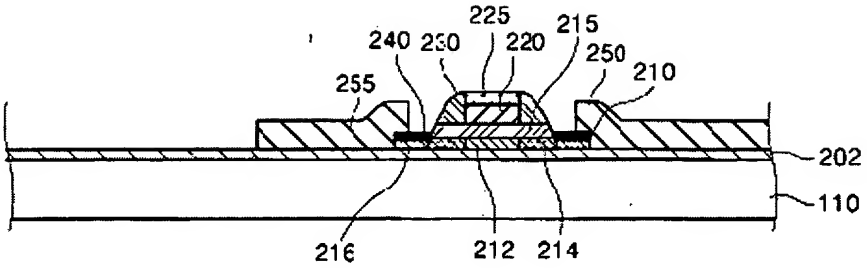


FIG.6M

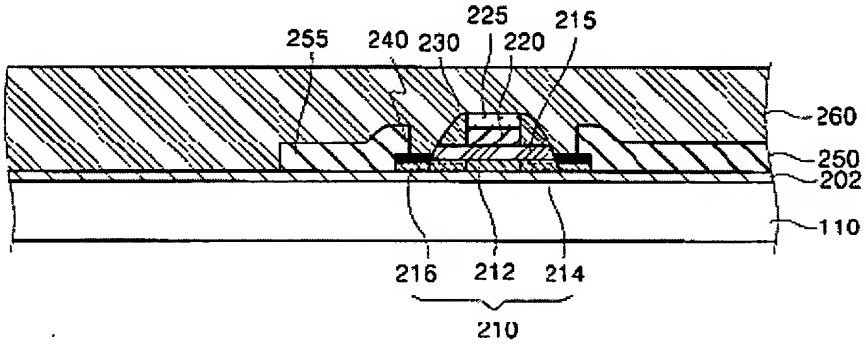


FIG.6N

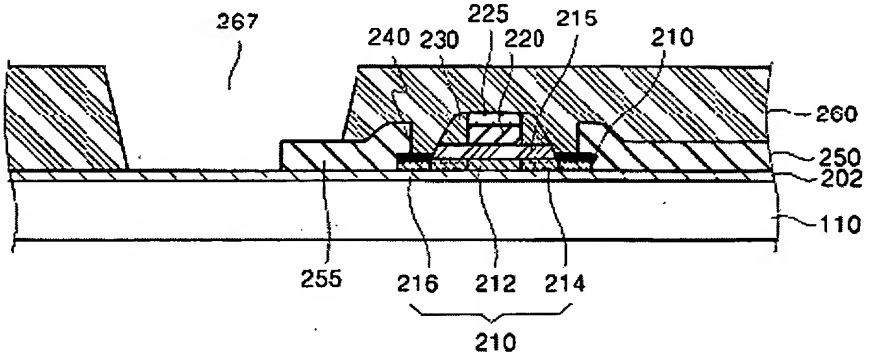


FIG.6O

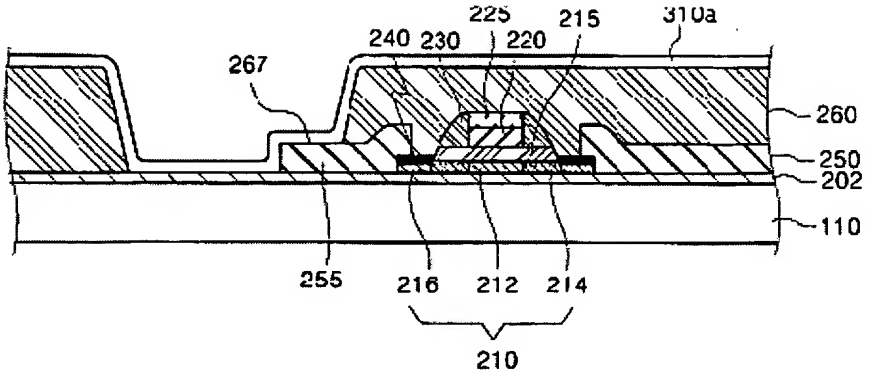


FIG.6P

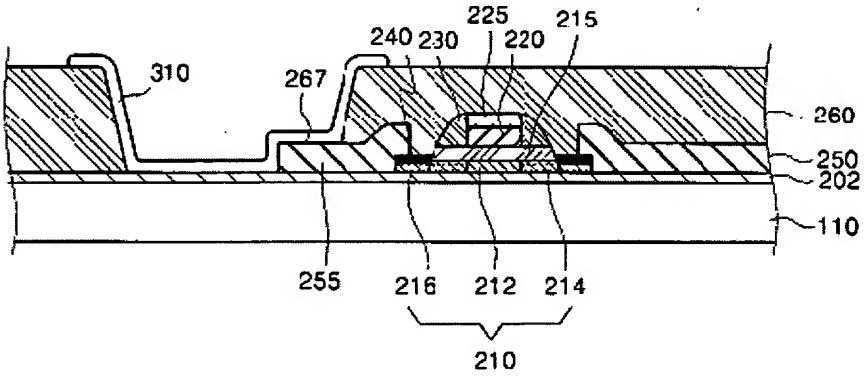


FIG.6Q

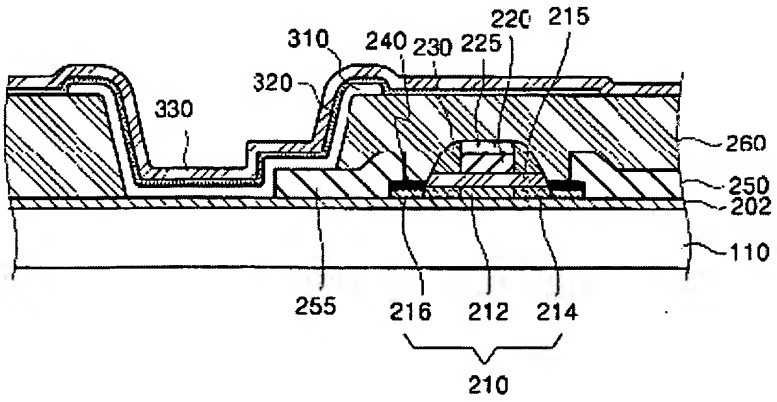


FIG.7

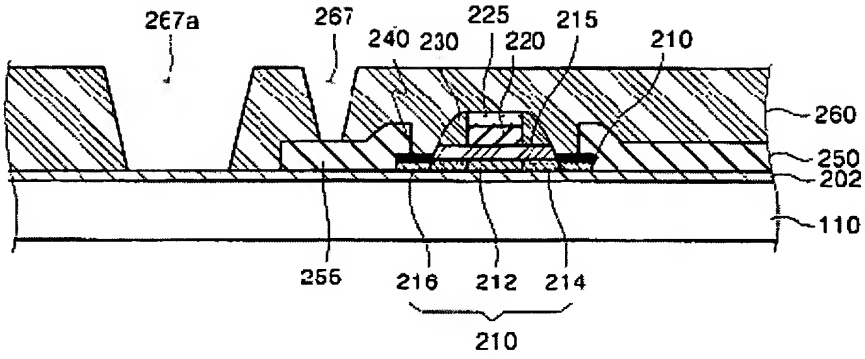


FIG.8

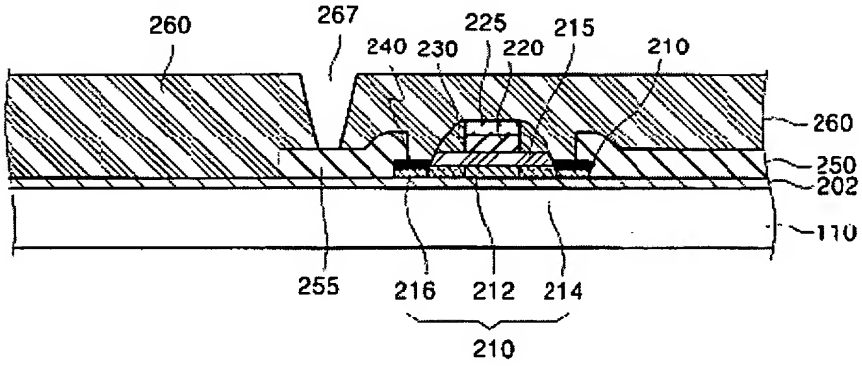


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FIG.9